FIGURE 1

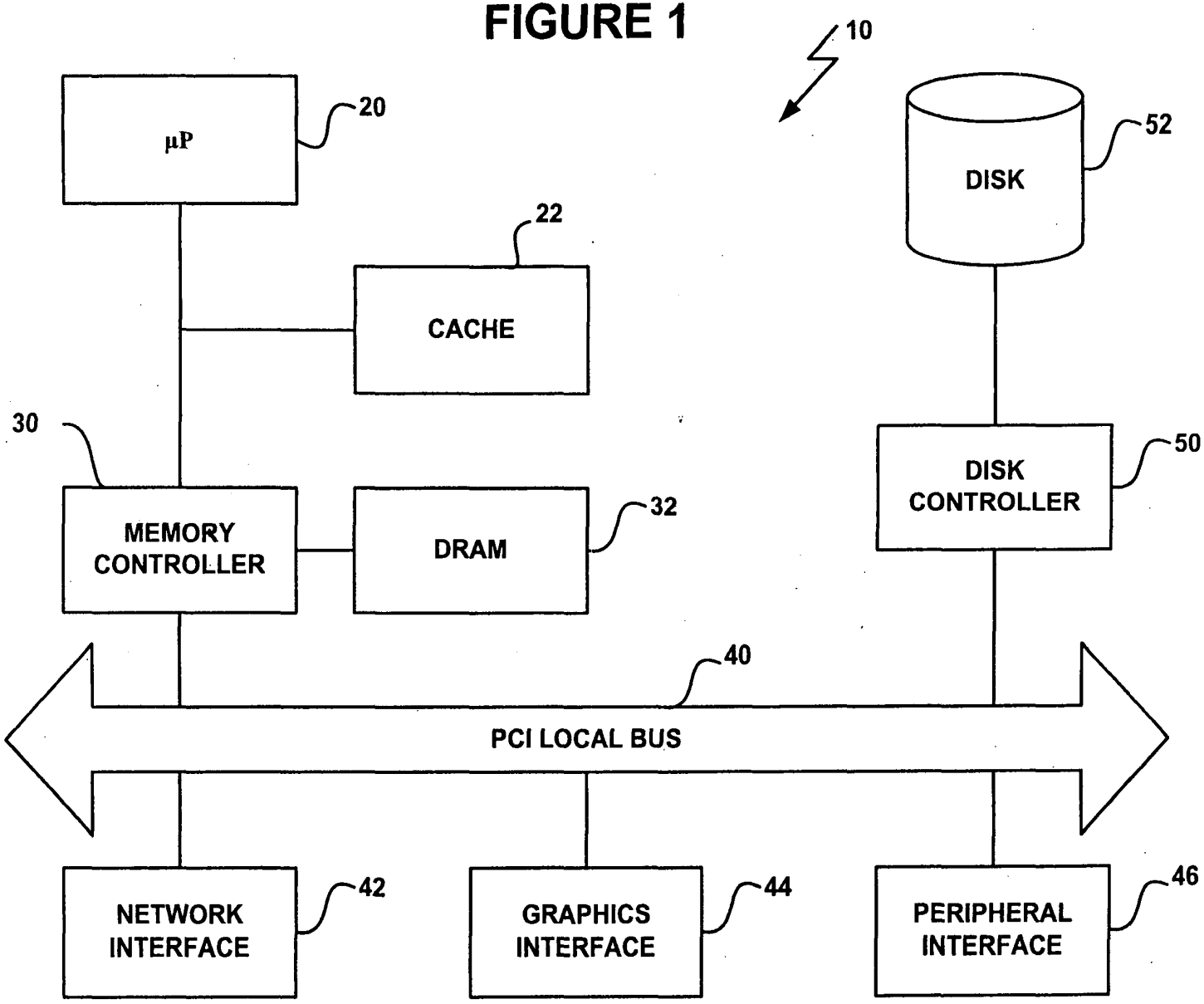

10
µP
20
DISK
52
22
CACHE
30
MEMORY CONTROLLER
DRAM
32
DISK CONTROLLER
50
40
PCI LOCAL BUS
NETWORK INTERFACE
42
GRAPHICS INTERFACE
44
PERIPHERAL INTERFACE
46

FIGURE 2

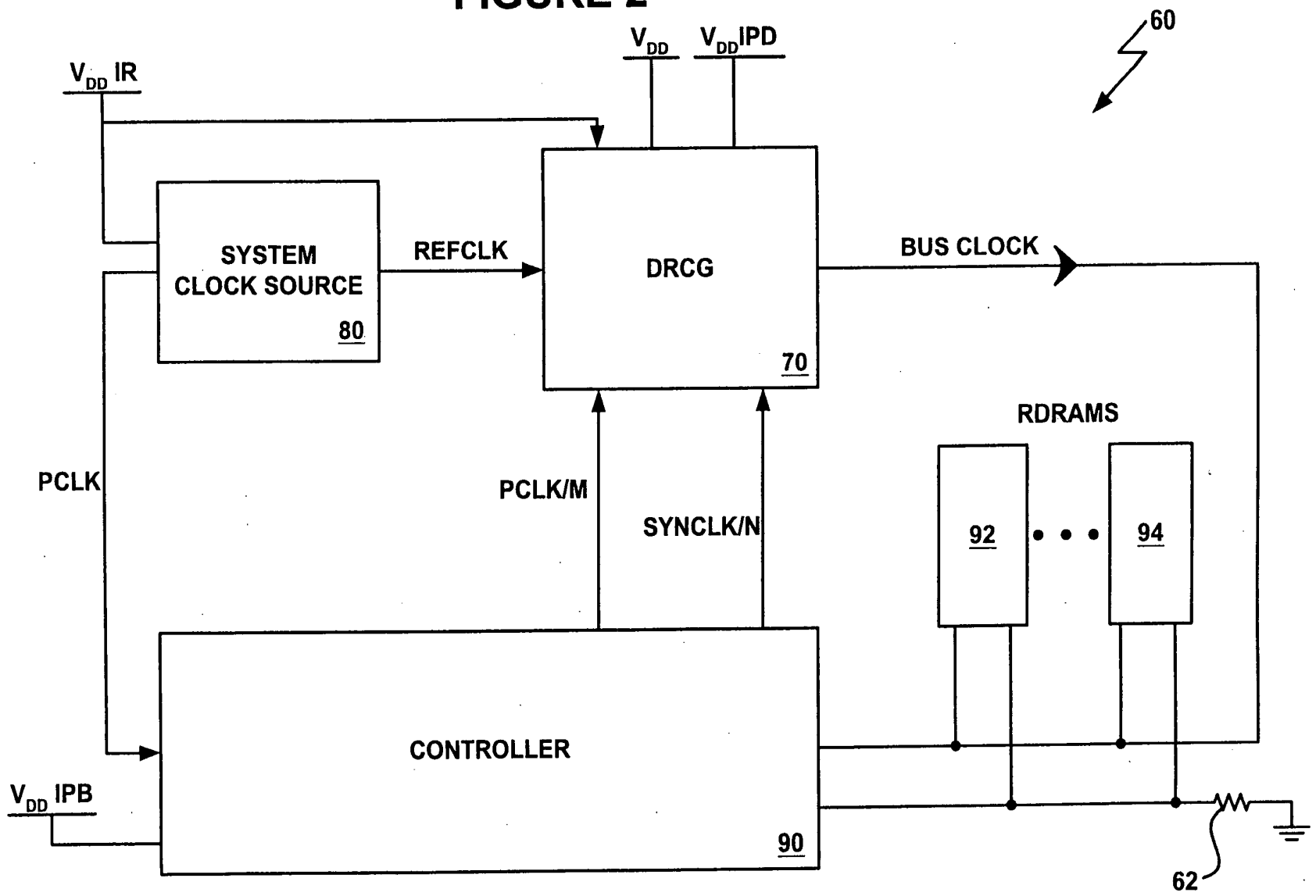
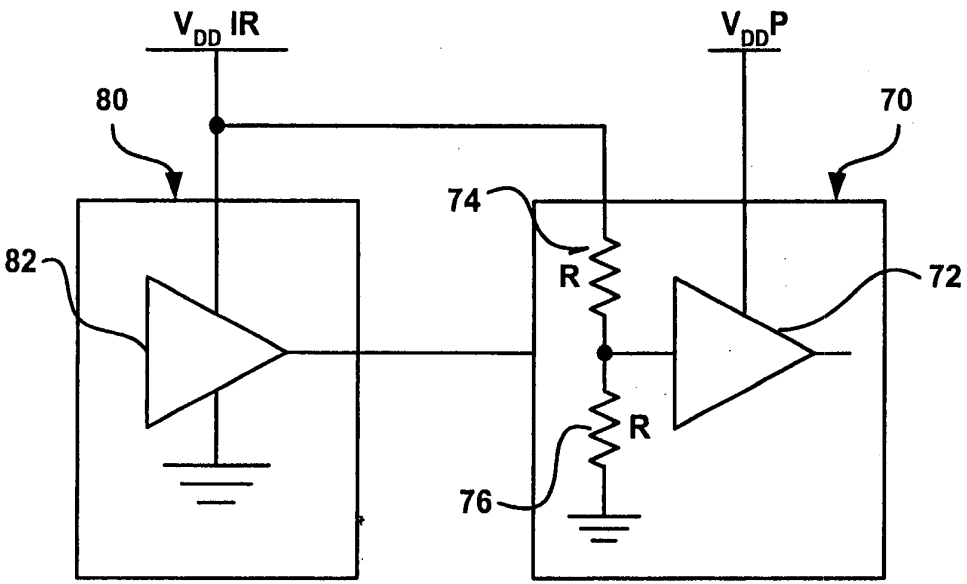

60
V_{DD}
V_{DD}IPD
V_{DD} IR
SYSTEM CLOCK SOURCE
80
REFCLK
DRCG
70
BUS CLOCK
RDRAMS
PCLK
PCLK/M
SYNCLK/N
92
94
CONTROLLER
V_{DD} IPB
90
62

FIGURE. 3



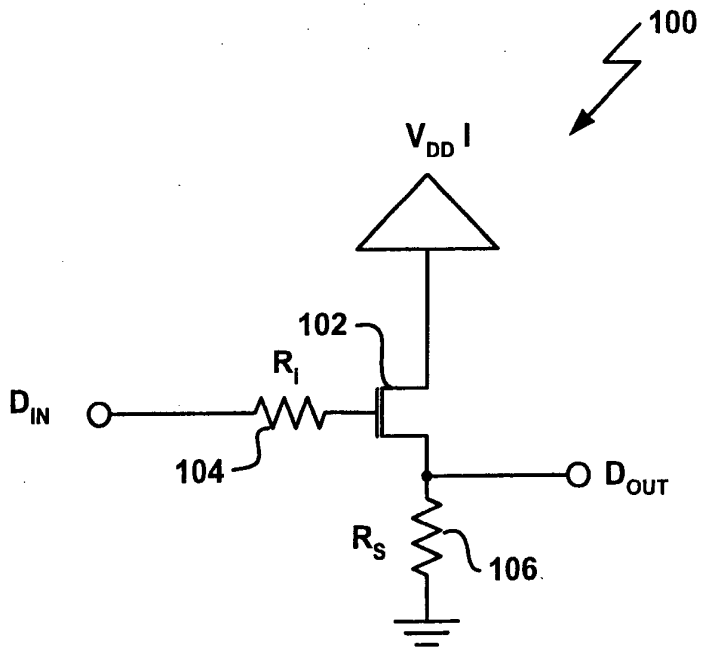


FIGURE 4

FIGURE 5

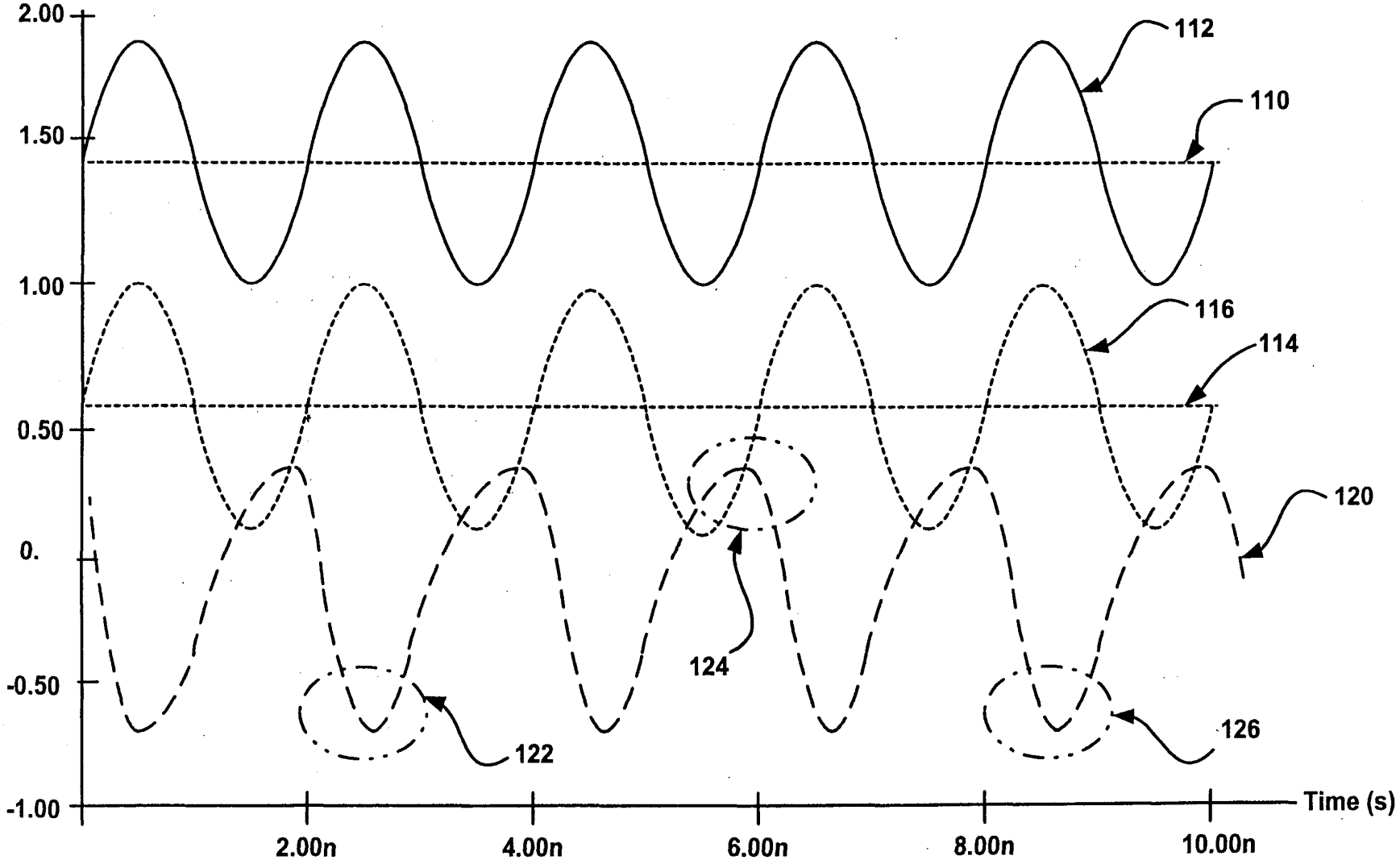

2.00
1.50
1.00
0.50
0.
-0.50
-1.00
2.00n
4.00n
6.00n
8.00n
10.00n
Time (s)
112
110
116
114
120
122
124
126

FIGURE 6

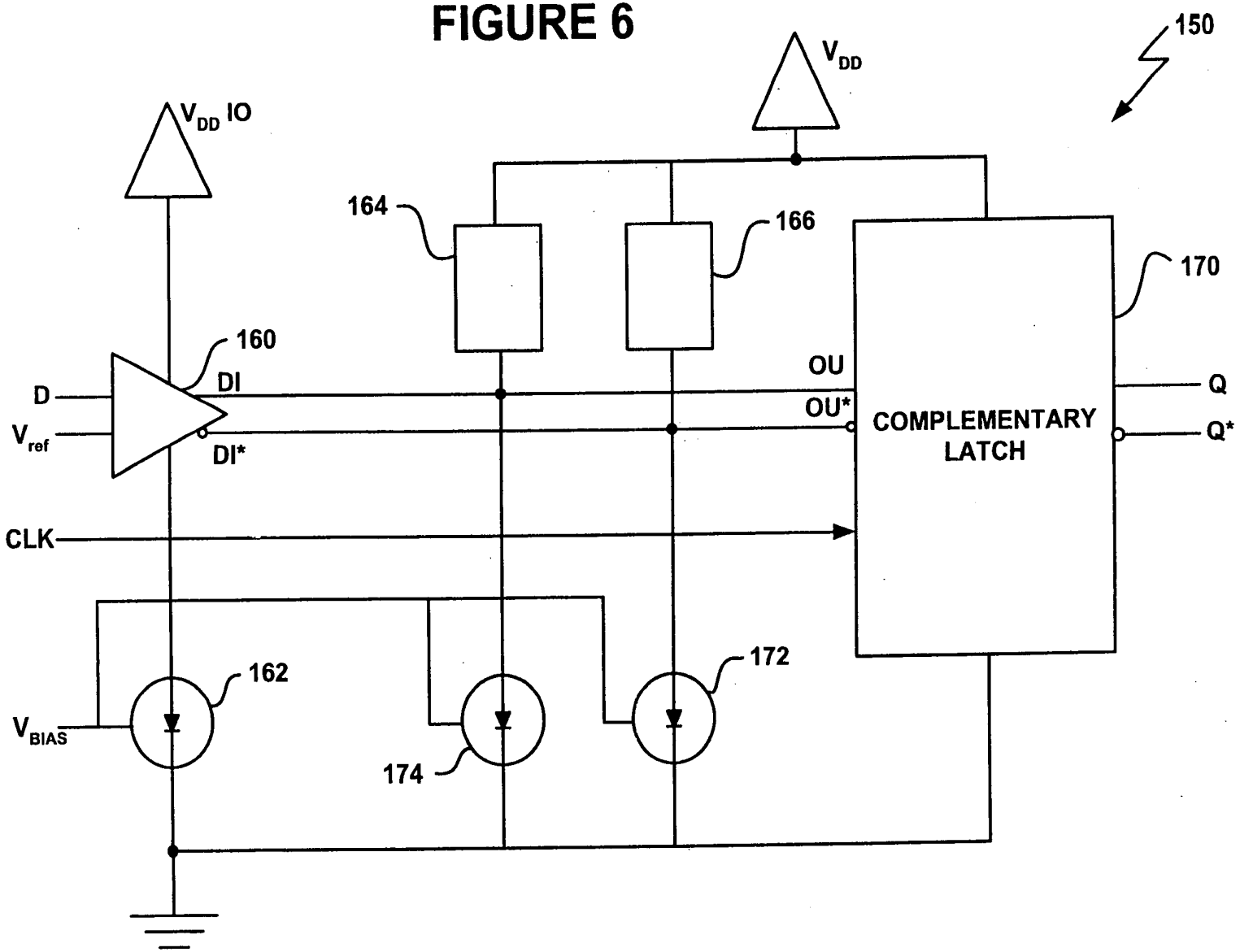
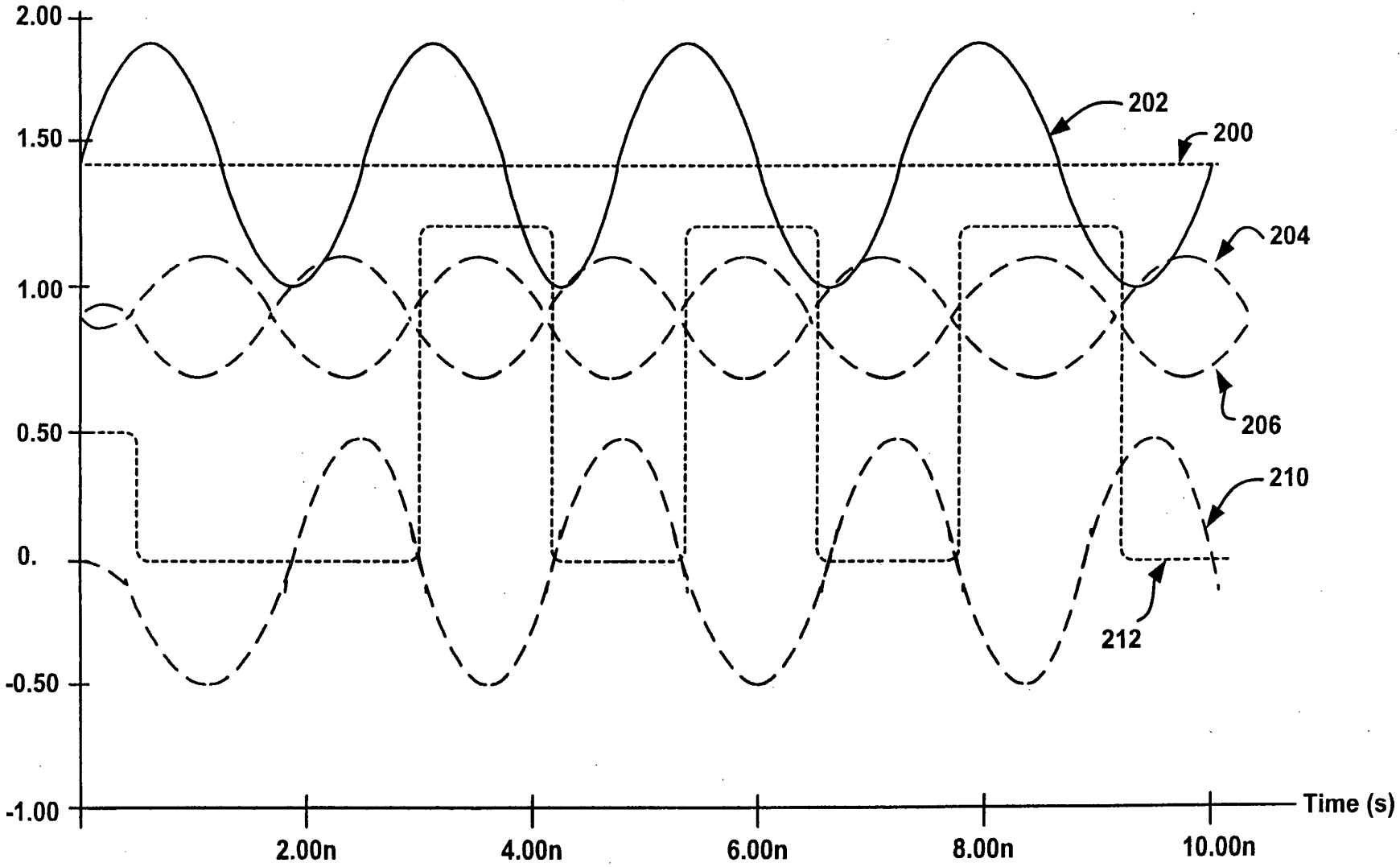

150
V_{DD}
V_{DD} IO
164
166
170
160
DI
D
V_{ref}
DI*
OU
OU*
COMPLEMENTARY LATCH
Q
Q*
CLK
162
172
V_{BIAS}
174

FIGURE 7


2.00
1.50
1.00
0.50
0.
-0.50
-1.00
2.00n
4.00n
6.00n
8.00n
10.00n
Time (s)
202
200
204
206
210
212

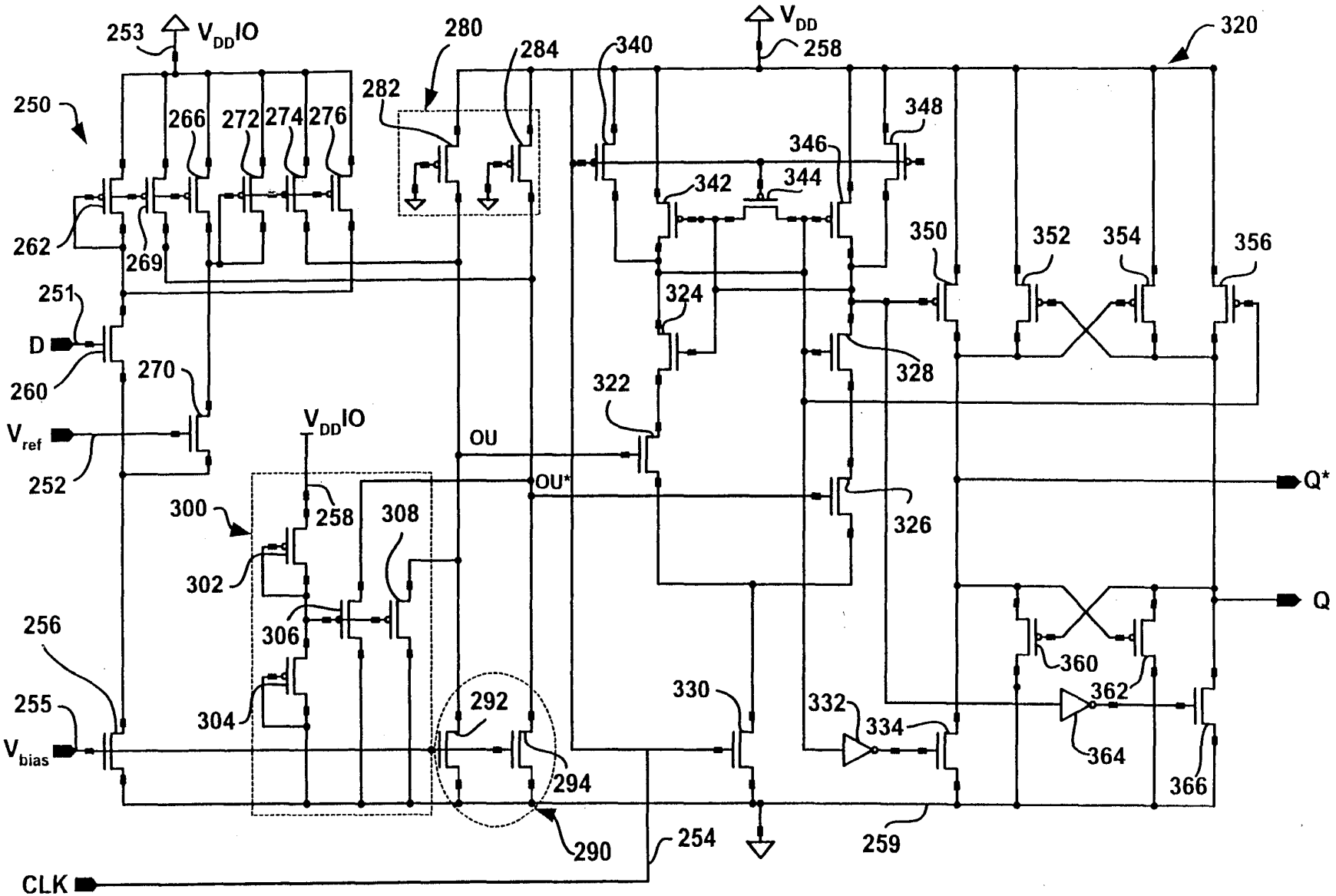

253
$V_{DD}IO$
280
284
340
V_{DD}
258
320
250
266
272
274
276
282
348
346
342
344
262
269
350
352
354
356
251
D
324
328
260
270
322
V_{ref}
$V_{DD}IO$
OU
252
OU*
Q*
300
258
308
326
302
306
Q
256
360
362
330
332
334
255
304
292
364
V_{bias}
294
366
290
254
259
CLK

FIGURE 8